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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,558	05/24/2005	Dietrich Mund	2133.065USU	4193
27623	7590	10/04/2007	EXAMINER	
OHLANDT, GREELEY, RUGGIERO & PERLE, LLP			COLEMAN, WILLIAM D	
ONE LANDMARK SQUARE, 10TH FLOOR			ART UNIT	PAPER NUMBER
STAMFORD, CT 06901			2823	
MAIL DATE		DELIVERY MODE		
10/04/2007		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/511,558	MUND ET AL.
	Examiner	Art Unit
	W. David Coleman	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 24 May 2005.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-42 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 42 is/are allowed.

6) Claim(s) 1-12,24-35 and 38 is/are rejected.

7) Claim(s) 13-22,36,37 and 39-41 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 05/05.

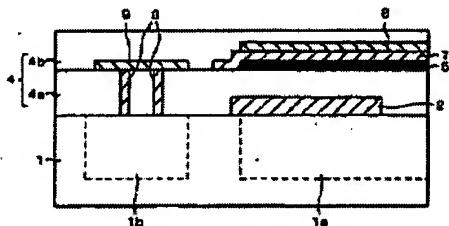
4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ .
5) Notice of Informal Patent Application
6) Other: ____ .

DETAILED ACTION

Claim Rejections - 35 USC § 102

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

1. Claims 1, 4, 5, 7, 8, 24, 25, 26, 27, 28, 31, 32 and 38 are rejected under 35 U.S.C. 102(a) as being anticipated by Matsumoto et al., European Patent Application Publication EP 1 178 529 A2.
2. Matsumoto discloses a semiconductor process as claimed. See FIGS. 1-16, where Matsumoto teaches the following limitations.



3. Matsumoto teaches a process for producing copy protection for an electronic circuit, comprising the steps of:

providing a substrate 1, having semiconductor structures 1a on at least a first side of the substrate;

providing a material 4a for coating the substrate; and

coating the substrate with a copy-protect layer by evaporation coating (please note that Matsumoto teaches forming the protective film with silicon oxide, silicon nitride or the like by plasma CVD and therefore the evaporation process is inherent in the vapor of the CVD plasma, also see paragraph [0035]).

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4. Pertaining to claim 4, Matsumoto teaches a process as claimed in claim 1, wherein the copy-protect layer is a continuous layer.

5. Pertaining to claims 5 and 28, Matsumoto teaches the process as claimed in claim 1, wherein the copy-protect layer comprises silicate glass (please note that silicon oxide is a form of silicate glass).

6. Pertaining to claims 7 and 31, Matsumoto teaches the process as claimed in claim 1, wherein the copy-protect layer comprises a binary system (please note that silicon oxide would meet this limitation).

7. Pertaining to claims 8 and 32, Matsumoto teaches the process as claimed in claim 1, wherein the copy-protect layer comprises a shield against electromagnetic waves (i.e., light shielding, because Matsumoto teaches a light blocking layer, this limitation has been met).

8. Pertaining to claim 24, Matsumoto teaches the electronic component with copy-protection, comprising:

an electronic circuit on a substrate having a first side;
semiconductor structures on the first side; and
a copy-protect layer fixedly joined to at least a region of the semiconductor structures.

9. Pertaining to claim 25, Matsumoto teaches the electronic component as claimed in claim 24, wherein the copy-protect layer comprises a first material, the first material being selected so that an etching process that dissolves the copy-protect layer destroys a portion of the electronic circuit.

10. Pertaining to claim 26, Matsumoto teaches the electronic component as claimed in claim 25, wherein the substrate comprises a semiconductor layer of silicon and the copy-protect layer comprises silicon.

11. Pertaining to claim 27, Matsumoto teaches the electronic component as claimed in claim 24, wherein the copy-protect layer is a continuous layer.

12. Pertaining to claim 35, Matsumoto teaches the electronic component as claimed in claim 24, further comprising connection structures and elevated connection structures arranged on a second side of the substrate, the second side being on the opposite side from the first side, wherein the elevated connection structures are electrically connected to the connection structures.

13. Pertaining to claim 38, Matsumoto teaches the electronic component as claimed in claim 24, further comprising connection structures and elevated connection contacts arranged on the first side of the substrate, the elevated connection contacts being electrically connected to the connection structures.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. Claims 2, 3, 6, 9, 10, 11, 12, 29, 30, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al., European Patent Application Publication EP 1 178 529 A2 in view of Camilletti et al., U.S. Patent 5,780,163.

16. Matsumoto discloses a semiconductor process substantially as claimed. Matsumoto teaches the process as claimed in claim 1, wherein the semiconductor structures, at least in regions, are covered by the copy-protect layer, the copy-protect layer being matched to the substrate so that an etching process dissolves the copy-protect layer. However, Matsumoto fails to teach the etching process also attacking the substrate so that the semiconductor structures are at least partially destroyed. Camilletti teaches a protective layer wherein etching of the protective layer also attacks the semiconductor structures and the substrate (see column 7, lines 17-25). In view of Camilletti, it would have been obvious to one of ordinary skill in the art to incorporate the features of Camilletti into the Matsumoto semiconductor process because the process will inhibit examination and/or reverse engineering of the underlying electronic or microelectronic device (see column 1, lines 13-17).

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17. Pertaining to claim 3, Matsumoto in view of Camilletti teaches the process as claimed in claim 2, wherein the substrate comprises a semiconductor layer of silicon and the copy-protect layer comprises silicon.

18. Pertaining to claims 6 and 29, Matsumoto in view of Camilletti teaches the process as claimed in claim 1, wherein the copy-protect layer comprises borosilicate glass with aluminum oxide and alkali metal oxide fractions (see column 7, line 5 where Camilletti teaches borides and potassium which is an alkali metal).

19. Pertaining to claims 9, 30 and 33, Matsumoto in view of Camilletti teaches the process as claimed in claim 1, wherein coating the substrate with the copy-protect layer comprises evaporation induced by thermal evaporation or by electron beam evaporation (because Matsumoto teaches a chemical vapor deposition process and Camilletti teaches a particle beam process, this limitation has been met by the combined teachings as a prior art process).

20. Pertaining to claims 10 and 34, Matsumoto in view of Camilletti teaches the process as claimed in claim 1, wherein the copy-protect layer is applied to the substrate in a thickness of from 0.01 to 1000 um (please note that Matsumoto discloses a thickness of 2um, see paragraph [0035]).

21. Pertaining to claims 11 and 12 Matsumoto in view of Camilletti fails to teach the process wherein the bias temperature and pressure are disclosed as below 300°C and 10^{-3} to 10^{-7} mbar

respectively. Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller, Lacey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986)

Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Objections

22. Claims 13-22, 36-37 and 39-41 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Allowable Subject Matter

23. Claim 42 allowed.

24. The following is an examiner's statement of reasons for allowance: the prior art does not anticipate nor render obviousness an electronic component having a copy-protect layer and a decryption device.
25. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.
27. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

28. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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